Document Identifier: DSP2067

Date: 2024-06-04

Version: 1.0.0

PLDM CXL Memory Modeling

Supersedes: None

Document Class: Informational

Document Status: Published

Document Language: en-US

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13 CONTENTS

1 Foreword

The *PLDM CXL Memory Modeling (DSP2067)* was prepared by the Platform Management Communications Infrastructure (PMCI) Working Group of DMTF.

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1.1 Acknowledgments

DMTF acknowledges the following individuals for their contributions to this document:

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- Patrick Caporale — Lenovo
- Yuval Itkin — NVIDIA Corporation
- Eliel Louzoun — Intel Corporation
- Hemal Shah — Broadcom Inc.

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21 # 2 Introduction

22 This document describes a modeling scheme for CXL Memory using PLDM for Monitoring and Control DSP0248 semantics.

23 ## 2.1 Document conventions

24 ### 2.1.1 Typographical conventions

25 The following typographical conventions are used in this document:

- Document titles are marked in *italics*.
- ABNF rules are in monospaced font.

26 ### 2.1.2 ABNF usage conventions

27 Format definitions in this document are specified using ABNF (see RFC5234), with the following deviations:

- Literal strings are to be interpreted as case-sensitive Unicode characters, as opposed to the definition in RFC5234 that interprets literal strings as case-insensitive US-ASCII characters.

28 ### 2.1.3 Reserved and unassigned values

29 Unless otherwise specified, any reserved, unspecified, or unassigned values in enumerations or other numeric ranges are reserved for future definition by DMTF.

30 Unless otherwise specified, numeric or bit fields that are designated as reserved shall be written as 0 (zero) and ignored when read.

31 ### 2.1.4 Byte ordering

32 Unless otherwise specified, byte ordering of multi-byte numeric fields or bit fields is “Big Endian” (that is, the lower byte offset holds the most significant byte, and higher offsets hold lesser significant bytes).

3 Scope

This document defines example data models for implementing the above-described generic device management of CXL memory devices using PLDM for Platform Monitoring and Control DSP0248 semantics. This document establishes a common framework that can provide implementation consistency between a system's Management Controller and CXL memory devices connected to the system. While this document focuses on CXL cards with DIMM expansion slots and CXL modules with embedded memory, these data models are assumed to be extensible to a variety of physical implementations and should not be construed to be limited to the examples herein.

35

4 Normative references

36 The following referenced documents are indispensable for the application of this document. For dated or versioned references, only the edition cited (including any corrigenda or DMTF update versions) applies. For references without a date or version, the latest published edition of the referenced document (including any corrigenda or DMTF update versions) applies.

37 Unless otherwise specified, for DMTF documents this means any document version that has minor or update version numbers that are later than those for the referenced document. The major version numbers must match the major version number given for the referenced document.

38 DMTF DSP0236, *MCTP Base Specification, 1.3* https://www.dmtf.org/sites/default/files/standards/documents/DSP0236_1.3.X.pdf

39 DMTF DSP0240, *Platform Level Data Model (PLDM) Base Specification, 1.1* https://www.dmtf.org/sites/default/files/standards/documents/DSP0240_1.1.X.pdf

40 DMTF DSP0241, *Platform Level Data Model (PLDM) Over MCTP Binding Specification, 1.0* https://www.dmtf.org/sites/default/files/standards/documents/DSP0241_1.0.X.pdf

41 DMTF DSP0245, *Platform Level Data Model (PLDM) IDs and Codes Specification, 1.3* https://www.dmtf.org/sites/default/files/standards/documents/DSP0245_1.3.X.pdf

42 DMTF DSP0248, *Platform Level Data Model (PLDM) for Platform Monitoring and Control Specification, 1.2* https://www.dmtf.org/sites/default/files/standards/documents/DSP0248_1.2.X.pdf

43 DMTF DSP0249, *Platform Level Data Model (PLDM) State Sets Specification, 1.1* https://www.dmtf.org/sites/default/files/standards/documents/DSP0249_1.1.X.pdf

44 DMTF DSP0257, *Platform Level Data Model (PLDM) FRU Data Specification, 1.0* https://www.dmtf.org/sites/default/files/standards/documents/DSP0257_1.0.X.pdf

45 DMTF DSP0267, *Platform Level Data Model (PLDM) for Firmware Update Specification, 1.1* https://www.dmtf.org/sites/default/files/standards/documents/DSP0267_1.2.X.pdf

46 DMTF DSP2054, *Platform Level Data Model (PLDM) NIC Modeling Specification, 1.0* https://www.dmtf.org/sites/default/files/standards/documents/DSP2054_1.0.X.pdf

47 DMTF DSP2061, *PLDM Accelerator Modeling Specification, 1.0* https://www.dmtf.org/sites/default/files/standards/documents/DSP2061_1.0.X.pdf

48 IETF RFC2781, *UTF-16, an encoding of ISO 10646*, February 2000 https://www.ietf.org/rfc/rfc2781.txt

49 IETF RFC4122, *A Universally Unique IDentifier (UUID) URN Namespace*, July 2005 https://www.ietf.org/rfc/rfc4122.txt

50 IETF RFC4646, *Tags for Identifying Languages*, September 2006 https://www.ietf.org/rfc/rfc4646.txt

51 IETF RFC5234, *ABNF: Augmented BNF for Syntax Specifications, January 2008* https://datatracker.ietf.org/doc/html/rfc5234

52 IETF STD63, *UTF-8, a transformation format of ISO 10646* https://www.ietf.org/rfc/std/std63.txt

53 ISO 8859-1, *Final Text of DIS 8859-1, 8-bit single-byte coded graphic character sets — Part 1: Latin alphabet No.1,* February 1998

54 ISO/IEC Directives, Part 2, *Principles and rules for the structure and drafting of ISO and IEC documents* https://www.iso.org/sites/directives/current/part2/index.xhtml

55 JESD301-1A.02, *PMIC50x0 Power Management IC Standard* https://www.jedec.org/standards-documents/docs/jesd301-1a02-rev-185

5 Terms and definitions

In this document, some terms have a specific meaning beyond the normal English meaning. Those terms are defined in this clause.

The terms “shall” (“required”), “shall not”, “should” (“recommended”), “should not” (“not recommended”), “may”, “need not” (“not required”), “can” and “cannot” in this document are to be interpreted as described in ISO/IEC Directives, Part 2, Clause 7. The terms in parentheses are alternatives for the preceding term, for use in exceptional cases when the preceding term cannot be used for linguistic reasons. Note that ISO/IEC Directives, Part 2, Clause 7 specifies additional alternatives. Occurrences of such additional alternatives shall be interpreted in their normal English meaning.

The terms “clause”, “subclause”, “paragraph”, and “annex” in this document are to be interpreted as described in ISO/IEC Directives, Part 2, Clause 6.

The terms “normative” and “informative” in this document are to be interpreted as described in ISO/IEC Directives, Part 2, Clause 3. In this document, clauses, subclauses, or annexes labeled “(informative)” do not contain normative content. Notes and examples are always informative elements.

Refer to DSP0240 for terms and definitions that are used across the PLDM specifications.

6 Symbols and abbreviated terms

Refer to DSP0240 and DSP0248 for symbols and abbreviated terms that are used across the PLDM specifications. For the purposes of this document, the following additional symbols and abbreviated terms apply.

CMB

CXL Memory Board

CMD

CXL Memory Device

CMM

CXL Memory Module

DIMM

Dual In-line Memory Module

PCB

Printed Circuit Board

PMIC

Power Management Integrated Circuit

76 # 7 PLDM CXL Memory Device Modeling overview

77 This document describes two hierarchical modeling schemes for CXL Memory Devices using PLDM for Platform Monitoring and Control DSP0248 semantics:

- CXL Memory Board (CXL Memory Device with DIMM Expansion)
- CXL Memory Module (CXL Memory Device with Embedded Memory)

78 The term CXL Memory Device is used to refer to both models. The models are scalable and allow consistent modeling of CXL Memory Devices with different configuration options.

79 While PLDM for Platform Monitoring and Control DSP0248 is a published standard, using the models defined in this document simplifies interoperability by establishing a consistent schema.

80 The basic format used for sending PLDM messages is defined in DSP0240. The format used for carrying PLDM messages over a transport-layer protocol and medium is given in companion documents to the base specification. For example, DSP0241 defines how PLDM messages are formatted and sent using MCTP as the transport.

81 The model supports the following:

- Consistent modeling of a CXL memory device regardless of the specific configuration and resource count
- CXL memory device hardware structure description
- Reporting of configuration changes such as firmware update

82 ## 7.1 Model Elements

83 ### 7.1.1 PLDM terminus

84 PLDM for Platform Monitoring and Control DSP0248 defines a single root for every device instance, referred to as a PLDM Terminus and identified with a TID. Throughout this document, the term **MC** is used to identify a PLDM terminus that communicates with a CXL Memory Controller on the device.

85 When there are multiple CXL Memory Controllers assembled on the same device, there may be a single CXL Memory Controller that reports all the sensors of all the elements on the CXL Memory Device to the MC. Alternatively, each CXL Memory Controller in the CXL Memory Device may present a separate PLDM terminus.

86 PLDM for Platform Monitoring and Control DSP0248 does not allow associating components reported via different PLDM termini since every database is relative to a given PLDM terminus. To overcome this constraint, the implementers can retrieve a globally unique ID (Board part number and serial number) from each TID and recognize these TIDs as belonging to the same CXL Memory Device. The process to retrieve the globally unique ID (Board part number and serial number) from each TID is out of scope for this document.

87 All PLDM IDs specified by the models in this document shall be consistent across all TIDs on a given card. This avoids conflict from duplication of IDs in the combined model, generated by merging the TID-specific model elements reported as part of the overall model.

7.1.2 CXL Memory Board (CMB)

In this model, the CXL Memory Board is a top-level element of the hierarchy containing one or more CXL Memory Controllers on a PCB. The CMB is a hardware solution that provides volatile and/or non-volatile Host-managed Device Memory (HDM) using CXL semantics and has one or more Memory Slots where DIMMs can be inserted. The CMB in this document refers to various form factors and is represented with PLDM Entity ID code 65 for **Memory Board**. CMB may contain sensors such as temperature, power-consumption, and health state.

7.1.3 CXL Memory Module (CMM)

In this model, the CXL Memory Module (CMM) is a top-level element of the hierarchy containing one or more CXL Memory Controllers on a PCB. The CMM is a hardware solution that provides volatile and/or non-volatile Host-managed Device Memory (HDM) using CXL semantics. The CMM in this document refers to various form factors and is represented with PLDM Entity ID code 66 for **Memory Module**. The CMM may contain sensors such as temperature, power-consumption, and health state.

7.1.4 CXL Memory Controller

In both hierarchy models above, the CXL Memory Controller is the second-level element of the hierarchy containing one or more sensors. A CXL Memory Controller is a hardware device whose main function is to provide host-access to its attached memory using CXL semantics. The CXL Memory Controller is represented with PLDM Entity ID code 143 for **Memory Controller** and may contain sensors such as power-consumption and temperature.

7.1.5 Power Management Integrated Circuit (PMIC)

The term PMIC in this document refers to the power management ICs (or voltage regulators) on a CXL Memory Device or on a DIMM that regulate power for the CXL Memory Controller and/or Memory Units. In this model, PMICs regulate the power for the CXL Memory Controller and other ancillary components at the second level of the hierarchy. PMICs exclusively regulating power for a memory Slot or Memory Module are considered to be at the third level of the hierarchy. PMICs are represented with PLDM Entity ID code 124 for **DC-DC converter** and may contain sensors such as fault state, power-consumption, current-consumption, and temperature.

7.1.6 Memory Slot

The term Memory Slot in this document represents the DIMM sockets mounted on the CXL Memory Board that allow the insertion of Memory Modules such as DIMMs. In the CMB model, the Memory Slot is considered to be at the second level of the hierarchy. The Memory Slot is represented with PLDM Entity ID code 186 for **Slot** and may contain sensors such as Presence Sensor.

7.1.7 Memory Module

The term Memory Module in this document refers to the DIMMs connected via Memory Slots present in the CMB. In

this model, the Memory Module is at the third level of the hierarchy. The Memory Module is represented with PLDM Entity ID code 66 for **Memory Module** and may contain other entities such as PMICs and sensors such as temperature.

7.1.8 Memory Media

The term Memory Media in this document refers to internal memory chips such as DRAM components, SRAM components, or NAND components present on the CMM or Memory Module (DIMM). In this model, the Memory Media soldered directly onto the CMM is considered to be at the second level of the hierarchy. Memory Media soldered onto a Memory Module (DIMM) that is inserted into a Memory Slot of the CMB is considered to be at the fourth level of the hierarchy. The Memory Media is represented with PLDM Entity ID code 142 for **Memory Chip**.

7.1.9 Memory Unit

The term Memory Unit in this document represents the logical entity such as Rank for DDR or Bank for HBM that is a Logical grouping of 1 to 40 Memory Medias (e.g., DRAM Die). The Memory Unit is represented with PLDM Entity ID code 11 for **Memory Rank**.

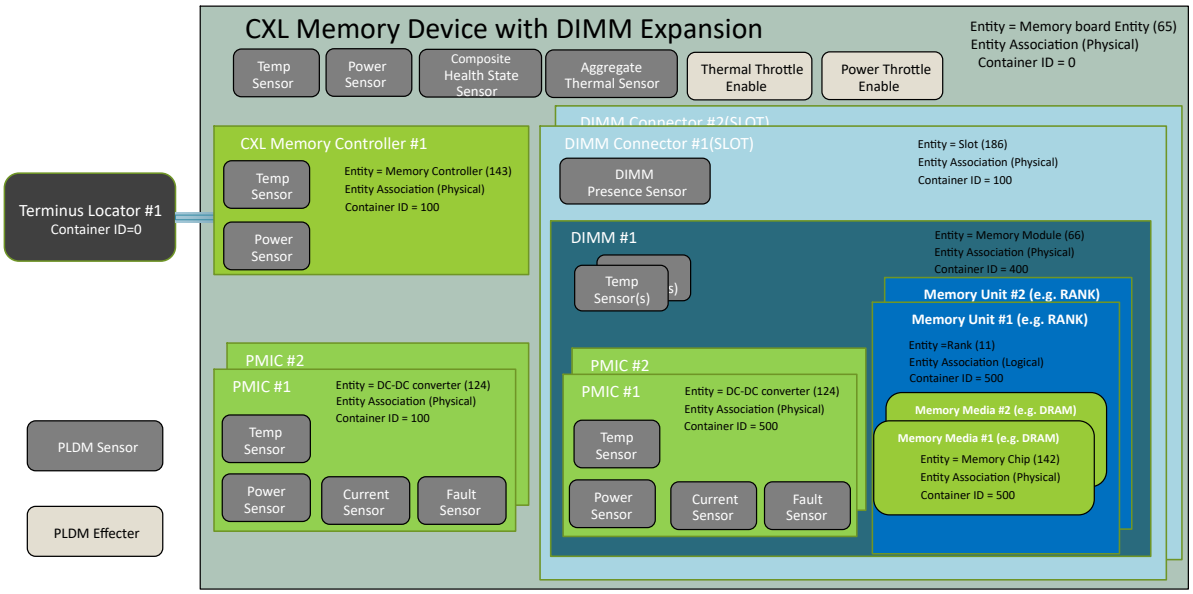
7.2 Model Sensors

7.2.1 Sensors Overview

Attributes are reported by means of sensors. Numeric sensors are used to report specific measured attributes. State sensors report operational and/or health state. The default thresholds for all numeric sensors shall be set by the hardware vendor. The sensors can be associated with any entity such as the CXL Memory Device or CXL Memory Controller. The description of each sensor is applicable only for the implemented sensors, and it is not mandatory to implement all the sensors described in this document. There may be auxiliary devices present on the CMD, and each auxiliary device may present its own set of sensors.

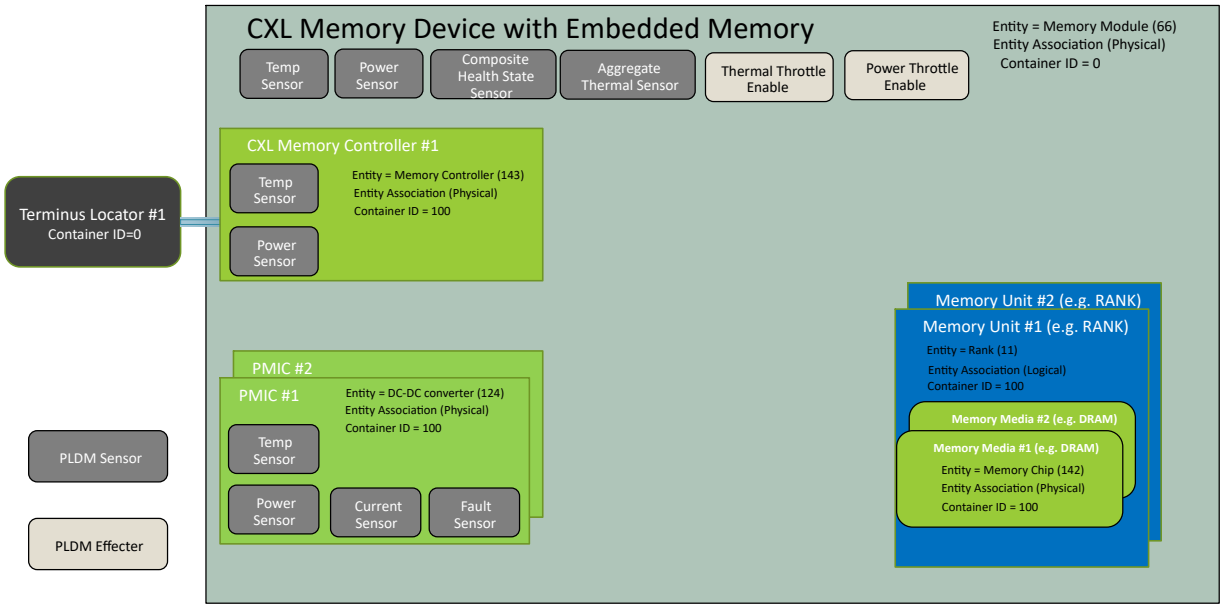
Note: The Sensor Auxiliary Names PDR is recommended for providing the proper name of each sensor.

108



109 **Figure 1 — CXL Memory Board (CMB) — PLDM model diagram**

110



111 **Figure 2 — CXL Memory Module (CMM) — PLDM model diagram**

7.2.2 CMD Temperature sensor

The temperature sensor on the CMD (both CMB and CMM) reports the card's ambient temperature and is represented using a numeric sensor. There may be multiple temperature sensors installed on the CMD. The sensor unit is 2 (Degrees C). Refer to the SensorUnits enumeration table in DSP0248.

7.2.3 CMD Power sensor

The power sensor on the CMD (both CMB and CMM) reports the estimated or measured aggregate power consumption of the CMD and is represented using a numeric sensor. A CMD that cannot accurately report its real-time power consumption may report its estimated maximal power. The sensor unit is 7 (Watts). Refer to the SensorUnits enumeration table in DSP0248.

7.2.4 CMD Composite state sensor

The CMD composite state sensor combines the following sensors.

1. CMD Thermal state sensor (Thermal Trip)
2. CMD health status sensor
3. CMD PMIC fault sensor status

7.2.5 CMD Aggregated temperature sensor

The temperature sensor on the CMD reports the consolidated temperature of all the subcomponents present in the devices, and it is represented using a numeric sensor. The sensor unit is 2 (Degrees C). Refer to the SensorUnits enumeration table in DSP0248. There may be multiple memory temperature sensors installed on the internal memory, on the soldered memory, and on the DIMMs.

Note: If temperature readings via the CXL Component Command Interface is implemented by the CMD, then the value of this temperature sensor should report out the same reading.

7.2.6 CMD Thermal Throttle Enable Effecter

The Thermal Throttle Enable Effecter on the CMD attempts to keep the running average temperature reading from all PLDM temperature sensors below their programmed thresholds by self-throttling device performance. The Set ID is 14 (Performance). Refer to Table 1 (General State Sets) in DSP0249.

7.2.7 CMD Power Throttle Enable Effecter

The Power Throttle Enable Effecter on the CMD attempts to keep the running average power reading from all PLDM power sensors below their programmed thresholds by self-throttling device performance. The Set ID is 14 (Performance). Refer to Table 1 (General State Sets) in DSP0249.

125 • 1 — Normal = Power throttling is not enabled.

126 • 2 — Throttled = Power throttling is enabled to keep all running average power sensor readings below their warning thresholds.

127 • 3 — Degraded = Power throttling is enabled to keep all running average power sensor readings below their critical thresholds.

128 7.2.8 CXL Memory Controller Temperature sensor

129 The temperature sensor on the CXL Memory Controller reports the internal ASIC temperature and is represented using a numeric sensor. The sensor unit is 2 (Degrees C). Refer to the SensorUnits enumeration table in DSP0248. The thresholds used by the sensor to define its normal, warning, critical, and fatal ranges are design-specific and should be defined by the device manufacturer.

130 7.2.9 CXL Memory Controller Power sensor

131 The power sensor on the CXL Memory Controller reports the estimated or measured aggregate power consumption of the CXL Memory Controller and is represented using a numeric sensor. A CXL Memory Controller that cannot accurately report its real-time power consumption may report its estimated maximal power. The sensor unit is 7 (Watts). Refer to the SensorUnits enumeration table in DSP0248. The thresholds that may be used by the sensor to define its normal, warning, critical, and fatal ranges are design-specific and should be defined by the device manufacturer.

132 7.2.10 PMIC Temperature sensor

133 The temperature sensor on the PMIC reports the Power Management IC temperature and is represented using a numeric sensor. The sensor unit is 2 (Degrees C). Refer to the SensorUnits enumeration table in DSP0248. The thresholds used by the sensor to define its normal, warning, critical, and fatal ranges are design-specific and should be defined by the device manufacturer.

134 7.2.11 PMIC Power sensor

135 The power sensor on the PMIC reports the estimated or measured aggregate power consumption of the subcomponents powered via the respective Power Management IC and is represented using a numeric sensor. A PMIC that cannot accurately report its real-time power consumption may report its estimated maximal power. The sensor unit is 7 (Watts). Refer to the SensorUnits enumeration table in DSP0248. The thresholds that may be used by the sensor to define its normal, warning, critical, and fatal ranges are design-specific and should be defined by the device manufacturer.

7.2.12 PMIC Current sensor

The current sensor on the PMIC reports the estimated or measured current consumption of the subcomponents powered via the respective Power Management IC and is represented using a numeric sensor. A PMIC that cannot accurately report its real-time power consumption may report its estimated maximal power. The sensor unit is 6 (Amps). Refer to the SensorUnits enumeration table in DSP0248. The thresholds that may be used by the sensor to define its normal, warning, critical, and fatal ranges are design-specific and should be defined by the device manufacturer.

7.2.13 PMIC Fault sensor

The Fault sensor on the PMIC reports its current power supply state since the last-known power cycle. The Set ID is 256 (Power Supply State). Refer to Table 9 (Power-Related State Sets) of DSP0249.

If PMIC implementations are based on JEDEC standard power management ICs, then the PLDM sensor state readings should follow the following mapping guidance shown in Table 1:

Table 1 — PMIC State Sensor Reading

Condition	PLDM State Set ID 256 Value	Description
VIN_BULK_OVER_VOLTAGE	7	Voltage Input out of Range
BUCK_OV_OR_UV	9	Power Out Failed/Lost
CRITICAL_TEMPERATURE	10	Thermal Trip

7.2.14 Memory Module Presence sensor

The Memory Module Presence sensor of the Memory Slot indicates whether a DIMM is present in the Slot / Connector or not and is represented using a State sensor. The Set ID is 13 (Presence). Refer to Table 1 (General State Sets) of DSP0249.

7.2.15 DIMM temperature sensor

The temperature sensor on the DIMM reports the DIMM ambient temperature and is represented using a numeric sensor. The sensor unit is 2 (Degrees C). Refer to the SensorUnits enumeration table in DSP0248. Sensor calibration and the thresholds used by the sensor to define its normal, warning, critical, and fatal ranges are design-specific and should be defined by the device manufacturer.

7.3 Hierarchy description of the CMD model elements

PLDM CMD Modeling uses a hierarchical model. Refer to section 10 PLDM associations and section 11 Entity Association PDR of DSP0248 to understand physical and logical associations.

148 ### 7.3.1 Physical Entity Association

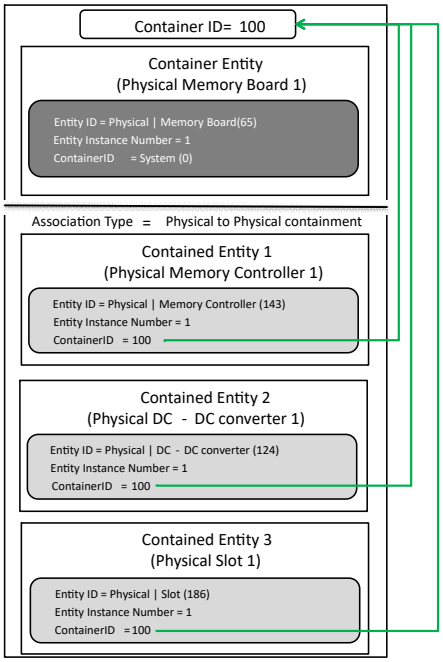
149 Physical association is defined in DSP0248 as a method to associate components that are physically connected to each other. The model uses this concept to describe the following structures:

- Content of the CXL Memory Device
- Content of the CXL Memory Controller
- Content of the PMIC
- Content of the Memory Slot
- Content of the Memory Module
- Content of the Memory Media

150 A hierarchy entity is defined using an entity association PDR identified with a unique ***ContainerID*** identifier parameter. The entity association PDR ***ContainerEntityContainerID*** references the PDR in which the entity is contained.

151 Figure 3 and 4 show the examples of how a CMD entity association PDR references its container entity and contained entities:

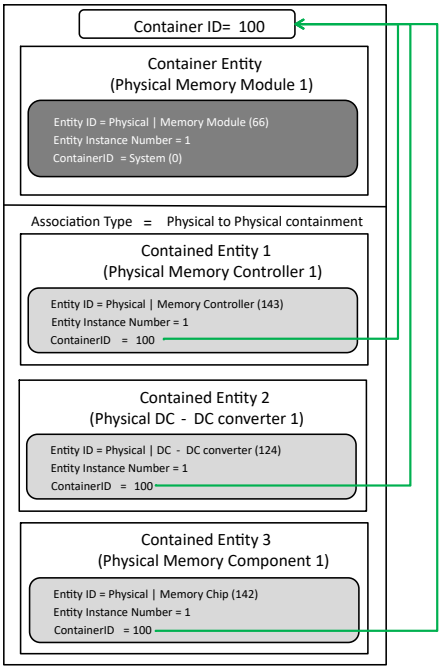
152



CXL Memory Board - Entity Association PDR		
Container ID		100
Container Entity – CXL Memory Board #1		
Entity Type	65	Memory Board
Entity Instance Number	1	
ContainerID	0	System
Association Type	Physical to Physical containment	
Contained Entity 1 - CXL Memory Controller #1		
Entity Type	143	CXL Memory Controller
Entity Instance Number	1	
ContainerID	100	CXL Memory Board #1
Contained Entity 2 – PMIC #1		
Entity Type	124	DC - DC converter
Entity Instance Number	1	
ContainerID	100	CXL Memory Board #1
Contained Entity 3 - DIMM Connector #1		
Entity Type	186	Slot
Entity Instance Number	1	
ContainerID	100	CXL Memory Board #1

153 **Figure 3 — Hierarchy description of a CMB using ContainerEntityContainerID referencing the ContainedEntityContainerID**

154



CXL Memory Module - Entity Association PDR		
Container ID		100
Container Entity – CXL Memory Module #1		
Entity Type	66	Memory Module
Entity Instance Number	1	
ContainerID	0	System
Association Type	Physical to Physical containment	
Contained Entity 1 - CXL Memory Controller #1		
Entity Type	143	CXL Memory Controller
Entity Instance Number	1	
ContainerID	100	CXL Memory Module #1
Contained Entity 2 – PMIC #1		
Entity Type	124	DC - DC converter
Entity Instance Number	1	
ContainerID	100	CXL Memory Module #1
Contained Entity 3 - Memory Component #1		
Entity Type	142	Memory Chip
Entity Instance Number	1	
ContainerID	100	CXL Memory Module #1

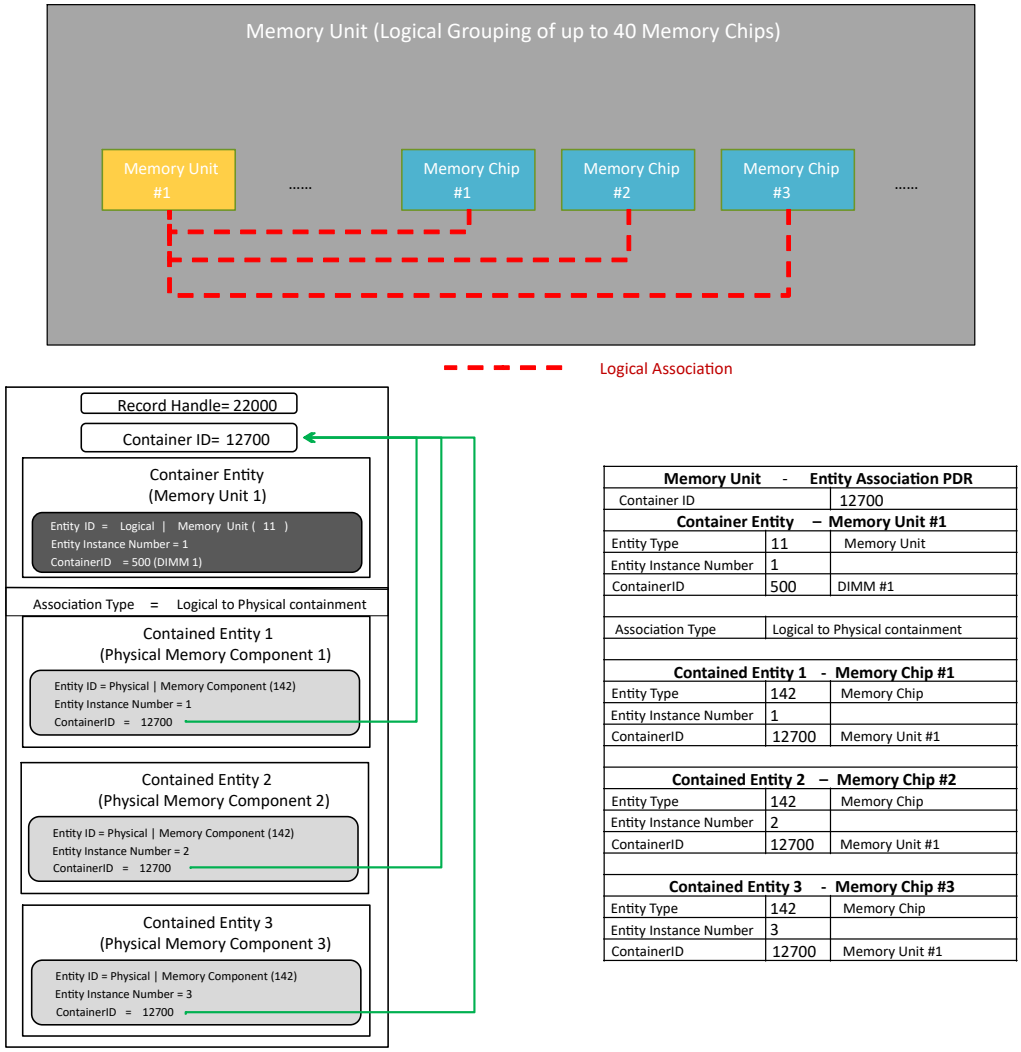
155 **Figure 4 — Hierarchy description of a CMM using ContainerEntityContainerID referencing the ContainedEntityContainerID**

156 7.3.2 Logical Entity Association

157 The DSP0248 defines logical association as a method to associate components which collectively form a shared property yet are not physically part of the same component. This type of association is typically used to group items that have a common parameter that is monitored or controlled. This model uses logical association to describe the following structures:

158 Figure 5 shows a logical association between the Memory Unit and a Memory Media:

159



Memory Unit - Entity Association PDR		
Container ID		12700
Container Entity – Memory Unit #1		
Entity Type	11	Memory Unit
Entity Instance Number	1	
ContainerID	500	DIMM #1
Association Type	Logical to Physical containment	
Contained Entity 1 - Memory Chip #1		
Entity Type	142	Memory Chip
Entity Instance Number	1	
ContainerID	12700	Memory Unit #1
Contained Entity 2 – Memory Chip #2		
Entity Type	142	Memory Chip
Entity Instance Number	2	
ContainerID	12700	Memory Unit #1
Contained Entity 3 - Memory Chip #3		
Entity Type	142	Memory Chip
Entity Instance Number	3	
ContainerID	12700	Memory Unit #1

160 **Figure 5 — Logical Containment PDR**

161 7.3.3 Sensor association

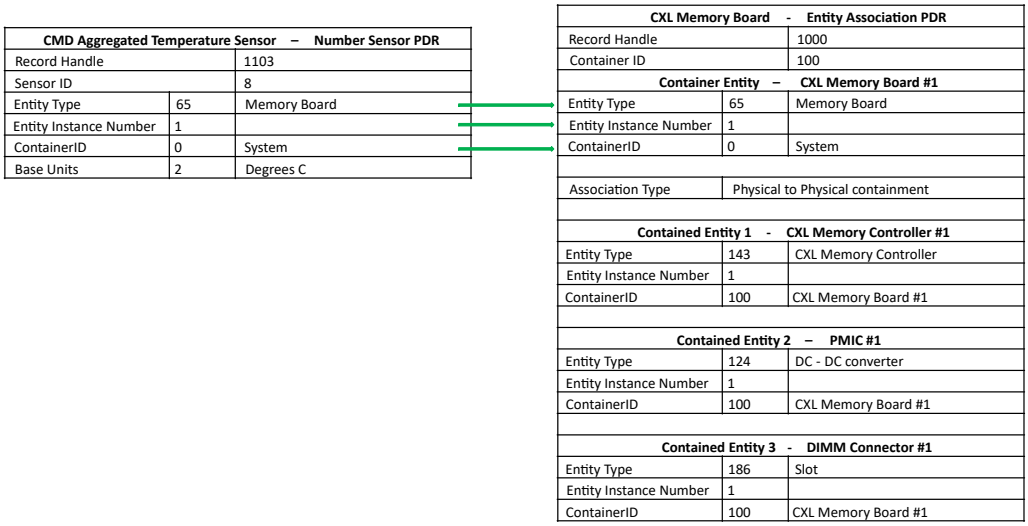
162 As per DSP0248, numeric and state sensors are not included inside entity association PDRs. They are instead associated with the measured entity by directly referencing the EntityContainerID, EntityType, and EntityInstanceNumber of the measured entity in an entity association PDR. A sensor is identified by a unique Sensor ID value.

163 7.3.3.1 Associating a sensor at the top level

164 When associating a sensor with the top-level entity, which is the system, the association uses the top-level ***ContainerEntityType, ContainerEntityInstanceNumber***, and **ContainerEntityContainerID** parameters.

165 Figure 6 illustrates the association of an Aggregated temperature sensor with the CXL Memory Device in the model.

166



167 **Figure 6 — Top-level sensor association**

168 7.4 Element PLDM Type IDs

169 The model uses the following Type ID for each component in the model, selected from the available types defined in DSP0249. Table 2 lists the chosen Type IDs used in the model:

170 **Table 2 — Entity IDs used in CXL Memory Model**

Component	PLDM Entity	Entity ID
CMB	Memory Board	65
CMM	Memory Module	66
CXL Memory Controller	Memory Controller	143
PMIC	DC-DC converter	124
Memory Slot **(e.g., DIMM Socket)**	Slot	186
Memory Module **(e.g., DIMM)**	Memory Module	66
Memory Media **(e.g., DRAM Die)**	Memory Chip	142
Memory Unit **(e.g., Rank)**	Memory Rank	11

7.5 Enumeration

PLDM for Platform Monitoring and Control DSP0248 uses enumerated IDs to define elements in the database. These IDs are labeled as:

- Container ID — unique for each container PDR in the model database
- Instance ID — unique for each entity type within a given hierarchy level
- Handle ID — unique ID for each PDR in the model database
- Sensor ID — unique for each sensor in the model database

The proposed model provides an example enumeration scheme for these IDs, allowing a reasonably scalable formulation. This model is only an example, and implementations should not rely on these values.

7.5.1 Enumeration scheme

The model assumes some maximal limits to define the enumerated values. These limits are provided as an example and can be adjusted according to the specific CXL Memory Device requirements.

The example model enumeration is designed to support a CXL Memory Device that does not exceed the following limits:

Table 3 — Enumeration Limits in CXL Memory Model

Component	Max Number of Instances
CXL Memory Controllers per CMD	4
PMICs per CMD / per DIMM	64
Memory Slots per CMB	16
Memory Media per DIMM / CMM	640
Memory Units per DIMM / CMM	16
Temperature Sensors per DIMM	10
Others	1

Note: If one of the above limits is insufficient for a CXL Memory Device, only the enumerated values will be affected, and the model structure will not have to change.

Figure 7 illustrates the enumeration scheme, calculated based on the above limits.

180

Item	Max Count	Base Container ID	Max Container ID	Base Handle	Max Handle	Base Sensor ID	Max Sensor ID	Base Instance	Max Instance	Type ID
CMB	1	100		1000	1000			1	1	65
CMM	1	100		1000	1000			1	1	66
CMD Temp Sensor	1			1100	1100	1	1	1	1	65 / 66
CMD Power Sensor	1			1101	1101	2	2	1	1	65 / 66
CMD Composite State Sensor	1			1102	1102	3	3	1	1	65 / 66
CMD Aggregated Temperature Sensor	1			1103	1103	4	4	1	1	65 / 66
CMD Thermal Throttle Enable Effecter	1			1104	1104	5	5	1	1	65 / 66
CMD Power Throttle Enable Effecter	1			1105	1105	6	6	1	1	65 / 66
CXL Controller	4	200	203	2000	2003			1	4	143
CXL Controller Temperature Sensor	4			2100	2103	10	13	1	4	143
CXL Controller Power Sensor	4			2200	2203	20	23	1	4	143
PMIC	64	300	363	3000	3063			1	64	124
PMIC Temperature Sensor	64			3100	3163	100	163	1	1	124
PMIC Power Sensor	64			3200	3263	200	263	1	1	124
PMIC Current Sensor	64			3300	3363	300	363	1	1	124
PMIC Fault Sensor	64			3400	3463	400	463	1	1	124
Memory Slot	16	400	415	4000	4015			1	16	186
Memory Module Presence Sensor	16			4100	4115	500	515	1	1	186
Memory Module	16	500	515	5000	5015			1	1	144
Memory Module Temperature Sensor	160			5100	5259	600	759	1	10	144
Memory Module - PMIC	1024	600	1623	6000	7023			1	64	124
Memory Module - PMIC Temperature Sensor	1024			7100	8123	700	1723	1	1	124
Memory Module - PMIC Power Sensor	1024			8200	9223	1000	2023	1	1	124
Memory Module - PMIC Current Sensor	1024			9300	10323	1300	2323	1	1	124
Memory Module - PMIC Fault Sensor	1024			10400	11423	1600	2623	1	1	124
CMM- Memory Chip	640	1700	2339	11500	12139	100	739	1	640	142
Memory Module - Memory Chip	10240	2400	12639	11500	21739			1	640	142
CMM Memory Unit	16	12700	12715	22000	22015			1	16	11
Memory Module Memory Unit	256	12800	13055	22000	22255			1	16	11

Calculated
Model Constant

181 **Figure 7 — Example Enumeration Scheme with Type IDs**

182 7.6 Model illustration

183 The CMD PLDM model is a hierarchical model. The following subclauses describe the model for each of the hierarchy levels:

184 7.6.1 CXL Memory Device

185 The top level of a CXL Memory Device may have the PCB card, CXL Memory Controllers, Memory Slots, Memory Modules, Memory chips, one or more Temperature sensors, composite state sensor, and power sensor. The PCB power consumption is represented with a power sensor. The CXL Memory Device operational state is represented by a composite state sensor. When there are multiple CXL Memory Controllers on the same card, CMD sensors are typically only reported by the first CXL Memory Controller. The CXL Memory Device is responsible for determining the order of CXL Memory Controllers in the card. Note that the top-level health state sensor of the composite state sensor may reflect the card-level sensors and the health states of PMICs and DIMMs.

7.6.2 CXL Memory Controller Hierarchy

The CXL Memory Controller hierarchy represents the active device (or one of multiple devices) that performs the CXL Memory Device control interface. The CXL Memory Controller is represented as a collection of sensors associated with it.

7.6.3 Memory Module Hierarchy

The Memory Module hierarchy represents the DIMMs connected via Memory Sockets present in the CMB. The Memory Module is represented as a collection of sensors associated with it.

7.6.4 Memory Media Hierarchy

The Memory Media hierarchy represents a memory chip component (or one of multiple components) that provides volatile and/or non-volatile host-managed device memory (HDM).

7.7 Events

This model supports using PLDM events as a method to notify the MC upon changes in the sensor readings/states as described in DSP0248. The following example events can be used with the model, and the implementation may choose to have more events.

7.7.1 CXL Memory Controller firmware version change

This event indicates to the MC that the firmware version of the CXL Memory Device has changed. The MC may use the ***GetPDRRepositoryInfo*** command and check if the ***timestamp*** parameter value has changed since it last read the PDRs. The MC may update the whole PDR repository by re-reading all the PDRs. The value used for the ***timestamp*** can be a virtual time value initialized by the CXL Memory Device at device initialization.

7.7.2 Health and State sensors events notifications

The sensors on the CXL Memory Device may report a change in value, health, or state using a PLDM state or numeric sensor event. Providing such a notification can significantly shorten the response time (compared to waiting for the MC to poll the sensors) for an occurrence that requires the MC to take action such as increasing the airflow from a cooling fan.

198 # 8 Model Use example

199 The following examples for modeling a CXL Memory Device using PLDM for Platform Monitoring and Control DSP0248 describes a CXL Memory Device with the following attributes:

200 Example 1:

- Single CXL Memory Board
  - Temperature Sensor
  - Power Sensor
  - Composite State Sensor
  - Aggregated Temperature Sensor
  - Thermal Throttle Enable Effecter
  - Power Throttle Enable Effecter
- Single CXL Memory Controller
  - Temperature Sensor
  - Power Sensor
- Single PMIC
  - Temperature Sensor
  - Power Sensor
  - Current Sensor
  - Fault Sensor
- Single DIMM Slot
  - Memory Module Presence sensor
- Single DIMM
  - Temperature Sensor
  - Single PMIC
    - Temperature Sensor
    - Power Sensor
    - Current Sensor
    - Fault Sensor
  - Dual Memory Chips on DIMM (logically grouped as a single Memory Unit)

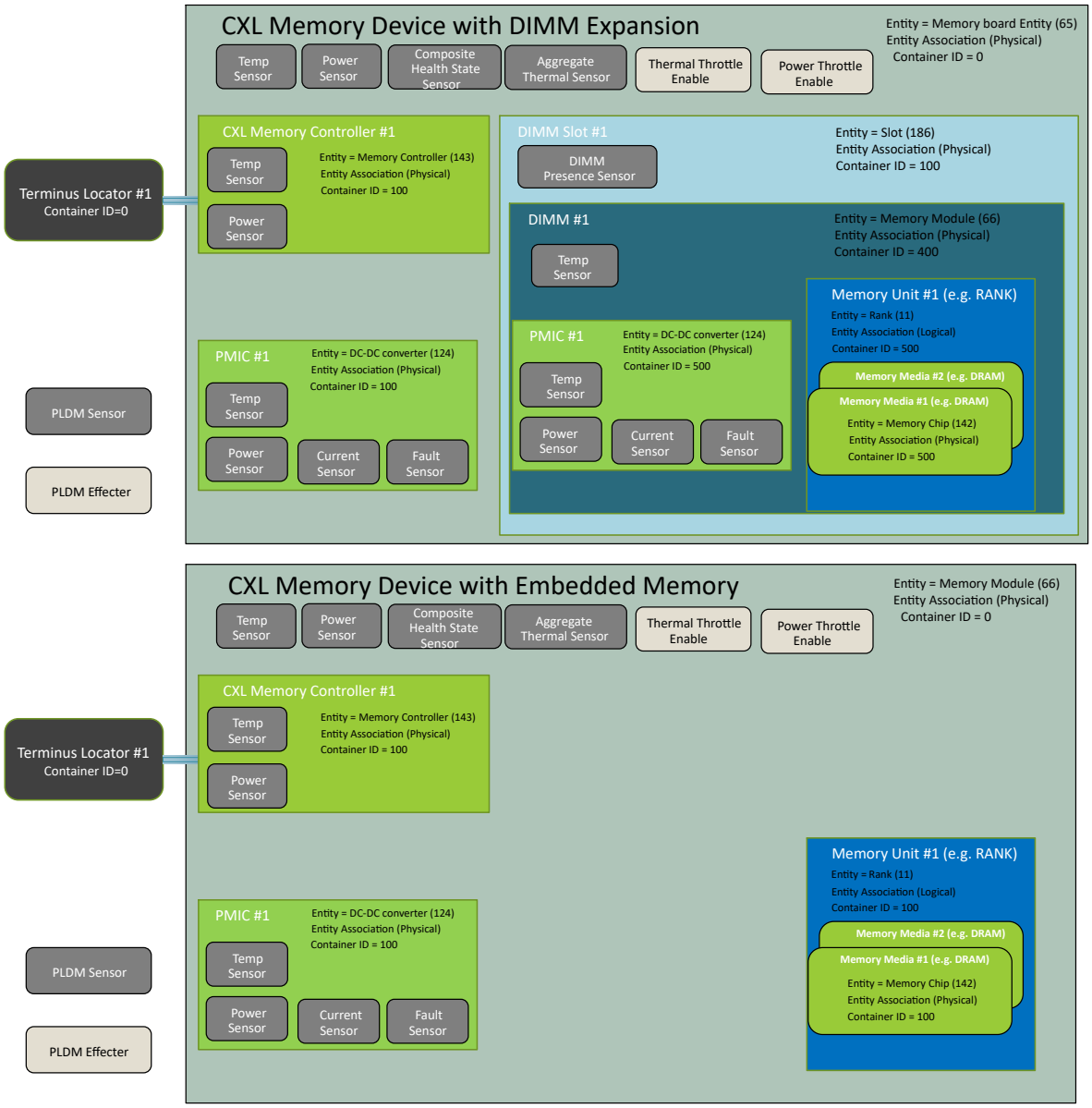
201 Example 2:

- Single CXL Memory Module
  - Temperature Sensor
  - Power Sensor
  - Composite State Sensor
  - Aggregated Temperature Sensor

    - Thermal Throttle Enable Effecter
    - Power Throttle Enable Effecter
- Single CXL Memory Controller
    - Temperature Sensor
    - Power Sensor
- Single PMIC
    - Temperature Sensor
    - Power Sensor
    - Current Sensor
    - Fault Sensor
- Dual Memory Chips (logically grouped as a single Memory Unit)

202 Figure 8 illustrates the model used in the examples.

203

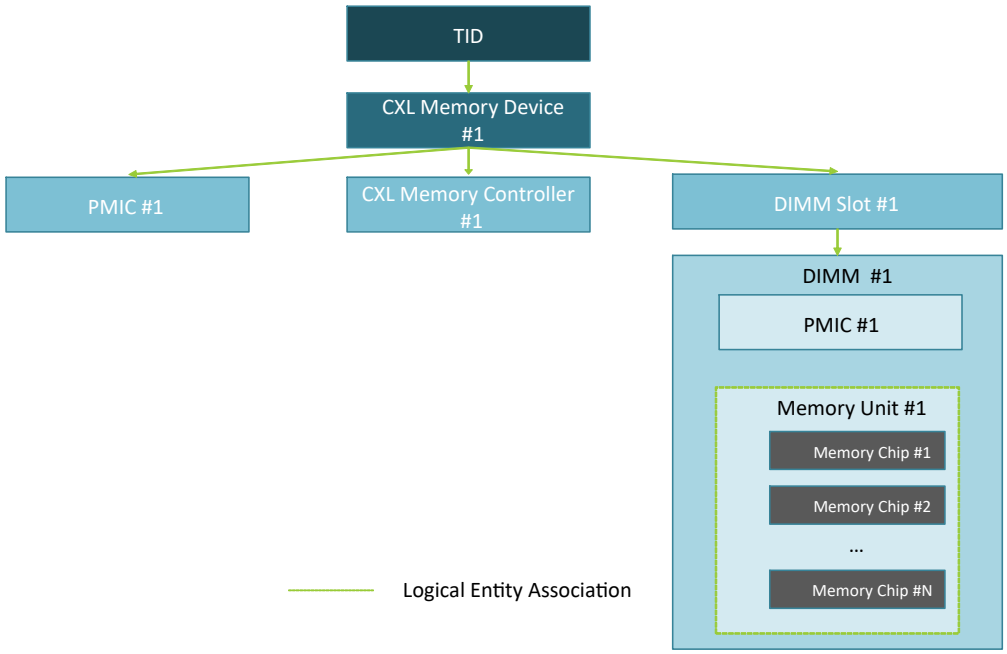


204 **Figure 8 — Example model diagrams**

205 8.1 Model hierarchy

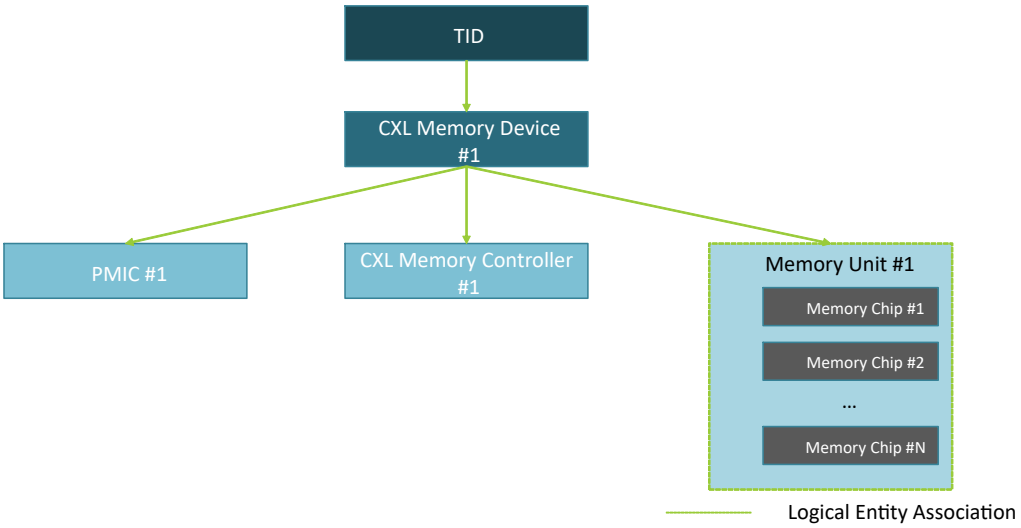
206 The model PDRs identify the elements depicted in Figure 6. The hierarchies are illustrated in the following diagram. For simplicity, Figure 9 and Figure 10 do not show the associated sensors.

207



208 **Figure 9 — CMB — Model hierarchy**

209



210 **Figure 10 — CMM — Model hierarchy**

211 ## 8.2 Top-level TID

212 The terminus ID is identified by the terminus locator PDR. The TID defines the top-level entry point to the PLDM model. Because there is only one CXL Memory Controller on the CXL Memory Device in this example, there is only one TID.

213 **Table 4 — TID PDR**

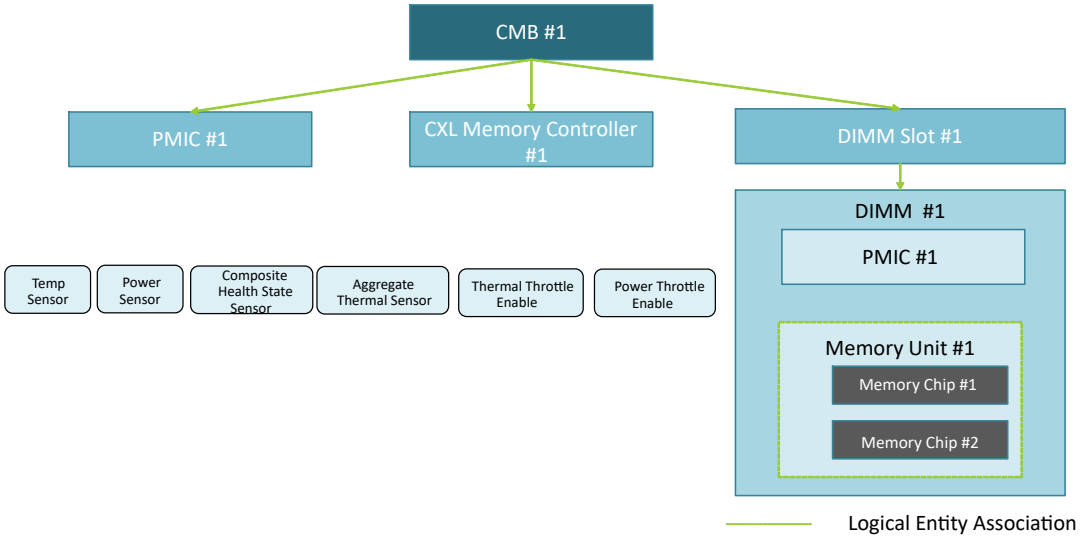
Field name	Value	Description
ContainerID	0	System
TID		Assigned by MC
RecordHandle	10	Opaque number
TerminusLocatorSize	1	Size of (EID) or size of (UID)
TerminusLocatorType	1	MCTP EID
EID	EID	MCTP assigned EID Value
UID	UID	Vendor-provided UUID format value

214 The TID value is assigned to the terminus by the MC. When the transport layer is MCTP, the identification of the terminus is performed using the Endpoint ID (EID) value. The UID value in the terminus locator PDR uses the device UUID value as the terminus UID. For more information regarding the terminus locator PDR, see DSP0248.

215 ## 8.3 CXL Memory Device Model

216 The top level of the model is the CXL Memory Device. The CXL Memory Device includes the physical elements, which include the CXL Memory Controller (only one CXL Memory Controller in this example), a PMIC, and memory chips (two memory chips in this example).

217



218 **Figure 11 — CMB level elements**

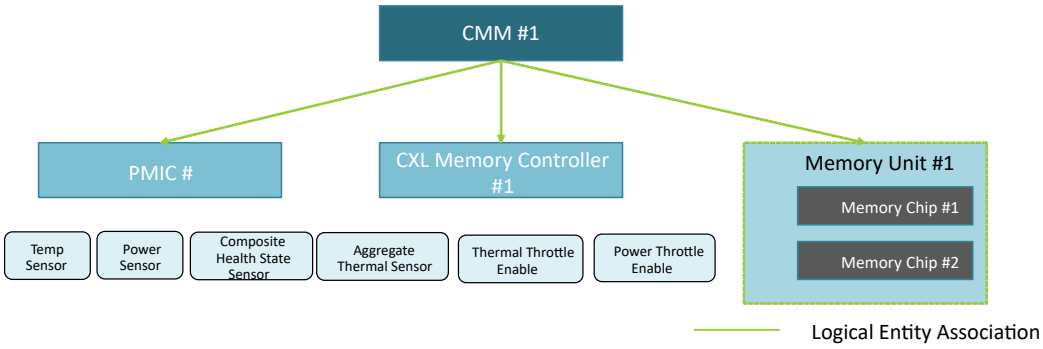
219 The sensors on the CXL Memory Device level are described using a reference to the measured entity, independent of the container that includes all the physical elements on the CXL Memory Device.

220

CXL Memory Board – Entity Association PDR		
Container ID		100
Container Entity – CXL Memory Board #1		
Entity Type	65	Memory Board
Entity Instance Number	1	
ContainerID	0	System
Association Type	Physical to Physical containment	
Contained Entity 1 – CXL Memory Controller #1		
Entity Type	143	CXL Memory Controller
Entity Instance Number	1	
ContainerID	100	CXL Memory Board #1
Contained Entity 2 – PMIC #1		
Entity Type	124	DC-DC converter
Entity Instance Number	1	
ContainerID	100	CXL Memory Board #1
Contained Entity 3- Memory Slot #1		
Entity Type	186	Slot
Entity Instance Number	1	
ContainerID	100	CXL Memory Board #1

221 **Figure 12 — CMB Container PDR**

222



223 **Figure 13 — CMM level elements**

224

CXL Memory Module – Entity Association PDR		
Container ID	100	
Container Entity – CXL Memory Module #1		
Entity Type	66	Memory Module
Entity Instance Number	1	
ContainerID	0	System
Association Type	Physical to Physical containment	
Contained Entity 1 – CXL Memory Controller #1		
Entity Type	143	CXL Memory Controller
Entity Instance Number	1	
ContainerID	100	CXL Memory Module #1
Contained Entity 2 – PMIC #1		
Entity Type	124	DC-DC converter
Entity Instance Number	1	
ContainerID	100	CXL Memory Module #1
Contained Entity 3 - Memory Media #1		
Entity Type	142	Memory Chip
Entity Instance Number	1	
ContainerID	100	CXL Memory Module #1
Contained Entity 4 – Memory Media #2		
Entity Type	142	Memory Chip
Entity Instance Number	2	
ContainerID	100	CXL Memory Module #1

225 **Figure 14 — CMM Container PDR**

226 In this example, note that the CXL Memory Device container ID, 100, is referenced by the sensors not included in the entity association PDR. The enumeration model shown in Figure 7 includes the container ID for every hierarchy level.

227 ### 8.3.1 CXL Memory Device Temperature Sensor PDR

228 **Table 5 — CMD Ambient Temperature Sensor PDR**

Field	Value	Description
RecordHandle	1100	
SensorID	1	
EntityType	65 / 66	Memory Board / Memory Module
EntityInstance	1	CXL Memory Device Instance #1
ContainerID	0	System
BaseUnit	2	Degrees C
UnitModifier	0	No need for scaling

229 ### 8.3.2 CXL Memory Device Power Sensor PDR

230 **Table 6 — CMD Power Sensor PDR**

Field	Value	Description
RecordHandle	1101	
SensorID	2	
EntityType	65 / 66	Memory Board / Memory Module
EntityInstance	1	CXL Memory Device Instance #1
ContainerID	0	System
BaseUnit	7	Watts
UnitModifier	-1	0.1 Watt resolution

231 ### 8.3.3 CXL Memory Device Composite State Sensor PDR

232 **Table 7 — CMD Composite State Sensor PDR**

Field	Value	Description
RecordHandle	1102	
SensorID	3	

Field	Value	Description
EntityType	65 / 66	Memory Board / Memory Module
EntityInstance	1	CXL Memory Device Instance #1
ContainerID	0	System
CompositeSensorCount	3	
SensorType	21	Thermal Trip
PossibleStates	Refer to Table 1 of DSP0249	
SensorType	1	Health state
PossibleStates	Refer to Table 1 of DSP0249	
SensorType	10	Operational Fault Status
PossibleStates	Refer to Table 1 of DSP0249	

233 ### 8.3.4 CXL Memory Device Aggregated Temperature Sensor PDR

234 **Table 8 — CMD Aggregated Temperature Sensor PDR**

Field	Value	Description
RecordHandle	1103	
SensorID	4	
EntityType	65 / 66	Memory Board / Memory Module
EntityInstance	1	CXL Memory Device Instance #1
ContainerID	0	System
BaseUnit	2	Degrees C
UnitModifier	0	No need for scaling

235 ### 8.3.5 CXL Memory Device Thermal Throttle Enable Effecter PDR

236 **Table 9 — CMD Thermal Throttle Enable Effecter PDR**

Field	Value	Description
RecordHandle	1104	
SensorID	5	
EntityType	65 / 66	Memory Board / Memory Module
EntityInstance	1	CXL Memory Device Instance #1
ContainerID	0	System
SensorType	14	Performance
PossibleStates	Refer to Table 1 of DSP0249	

237 ### 8.3.6 CXL Memory Device Power Throttle Enable Effecter PDR

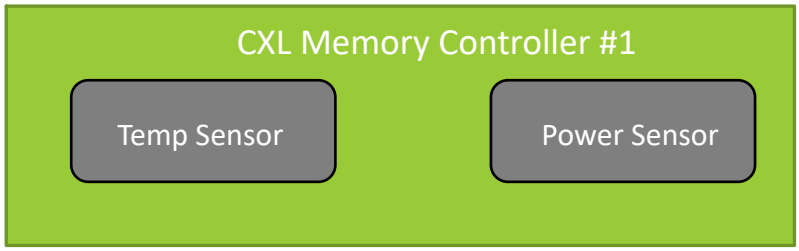
238 **Table 10 — CMD Power Throttle Enable Effecter PDR**

Field	Value	Description
RecordHandle	1105	
SensorID	6	
EntityType	65 / 66	Memory Board / Memory Module
EntityInstance	1	CXL Memory Device Instance #1
ContainerID	0	System
SensorType	14	Performance
PossibleStates	Refer to Table 1 of DSP0249	

239 ## 8.4 CXL Memory Controller Model

240 The CXL Memory Controller is the active device in charge of providing host-access to its attached memory using CXL semantics. Being a physical entity, the CXL Memory Controller is already declared within Figure 7. The content of the CXL Memory Controller includes a set of device-level sensors. The following diagram illustrates the model elements for the CXL Memory Controller in the example model:

241



242 **Figure 15 — Example model CXL Memory Controller**

243 The CXL Memory Controller content is declared using an entity-association PDR that includes the hierarchical description of the CXL Memory Controller. The device-level sensors are declared with separate PDRs using direct references to the measured entities.

244

CXL Memory Controller – Entity Association PDR		
Container ID	200	
Container Entity – CXL Memory Controller #1		
Entity Type	143	Memory Controller
Entity Instance Number	1	
ContainerID	100	CMB #1 / CMM #1
Association Type	Physical to Physical containment	

245 **Figure 16 — CXL Memory Controller Entity Association PDR**

246 ### 8.4.1 CXL Memory Controller Temperature Sensor PDR

247 **Table 11 — CXL Memory Controller Temperature Sensor PDR**

Field	Value	Description
RecordHandle	2100	
SensorID	10	
EntityType	143	Memory Controller
EntityInstance	1	
ContainerID	100	CMB #1 / CMM #1
BaseUnit	2	Degrees C

Field	Value	Description
UnitModifier	0	No need for scaling

248 ### 8.4.2 CXL Memory Controller Power Sensor PDR

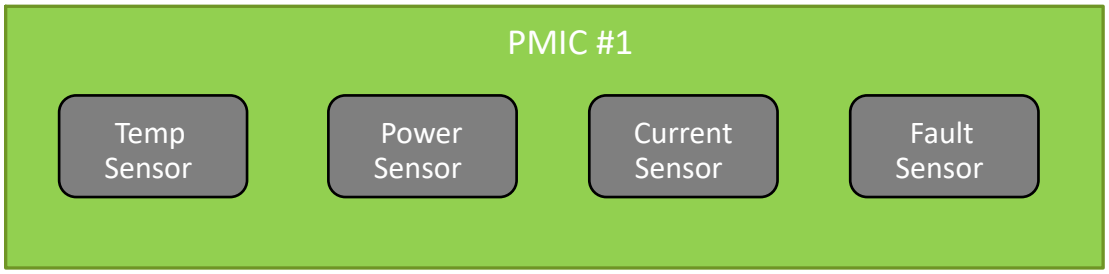
249 **Table 12 — CXL Memory Controller Power Sensor PDR**

Field	Value	Description
RecordHandle	2200	
SensorID	20	
EntityType	143	Memory Controller
EntityInstance	1	
ContainerID	100	CMB #1 / CMM #1
BaseUnit	7	Watts
UnitModifier	-1	0.1 Watt resolution

250 ## 8.5 PMIC

251 The power management IC (or voltage regulator) regulates power for the CXL Memory Controllers and/or Memory Units. Being a physical entity, the PMIC is already declared within Figure 7. The content of the PMIC includes a set of device-level sensors. The following diagram illustrates the model elements for the PMIC in the example model:

252



253 **Figure 17 — Example model PMIC**

254 The PMIC content is declared using an entity-association PDR that includes the hierarchical description of the PMIC. The device-level sensors are declared with separate PDRs using direct references to the measured entities.

255

PMIC – Entity Association PDR		
Container ID		300 / 600
Container Entity – PMIC #1		
Entity Type	124	DC-DC converter
Entity Instance Number	1	
ContainerID	100/400	CMB #1 / CMM #1 or DIMM #1
Association Type	Physical to Physical containment	

256 **Figure 18 — PMIC Entity Association PDR**

257 ### 8.5.1 PMIC Temperature Sensor PDR

258 **Table 13 — PMIC Temperature Sensor PDR**

Field	Value	Description
RecordHandle	3100/7100	
SensorID	100	
EntityType	124	DC-DC converter
EntityInstance	1	
ContainerID	100/400	CMB #1 / CMM #1 or DIMM #1
BaseUnit	2	Degrees C
UnitModifier	0	No need for scaling

259 ### 8.5.2 PMIC Power Sensor PDR

260 **Table 14 — PMIC Power Sensor PDR**

Field	Value	Description
RecordHandle	3200/8200	
SensorID	200	
EntityType	124	DC-DC converter
EntityInstance	1	

Field	Value	Description
ContainerID	100/400	CMB #1 / CMM #1 or DIMM #1
BaseUnit	7	Watts
UnitModifier	-1	0.1 Watt resolution

261 ### 8.5.3 PMIC Current Sensor PDR

262 **Table 15 — PMIC Current Sensor PDR**

Field	Value	Description
RecordHandle	3300/9300	
SensorID	300	
EntityType	124	DC-DC converter
EntityInstance	1	
ContainerID	100/400	CMB #1 / CMM #1 or DIMM #1
BaseUnit	6	Amps
UnitModifier	0	No need for scaling

263 ### 8.5.4 PMIC Fault Sensor PDR

264 **Table 16 — PMIC Fault Sensor PDR**

Field	Value	Description
RecordHandle	3400/10400	
SensorID	400	
EntityType	124	DC-DC converter
EntityInstance	1	
ContainerID	100/400	CMB #1 / CMM #1 or DIMM #1
SensorType	256	Power Supply State
PossibleStates	Refer to Table 1 of DSP0249	

8.6 DIMM Slot

DIMM Slot refers to one of the empty slots or sockets mounted on the CMB PCB that allow for the insertion of DIMMs. Being a physical entity, the DIMM Slot is already declared within Figure 7. The content of the DIMM Slot includes a set of device-level sensors. The following diagram illustrates the model elements for the DIMM Slot in the example model:

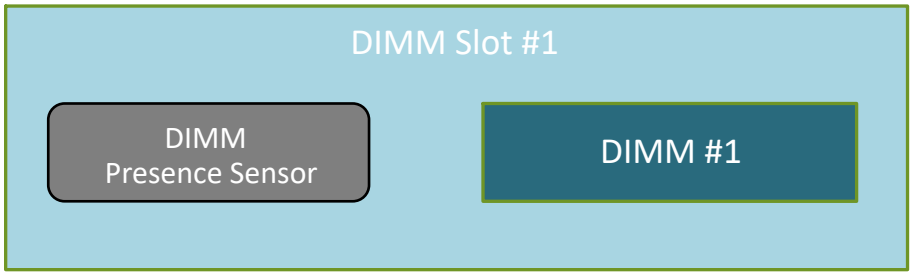


Figure 19 — Example model DIMM Slot

The DIMM Slot content is declared using an entity-association PDR that includes the hierarchical description of the DIMM Slot. The device-level sensors are declared with separate PDRs using direct references to the measured entities.

Memory Slot – Entity Association PDR		
Container ID		400
Container Entity – DIMM Slot #1		
Entity Type	186	Slot
Entity Instance Number	1	
ContainerID	100	CMB #1
Association Type	Physical to Physical containment	

Figure 20 — DIMM Slot Entity Association PDR

8.6.1 DIMM Presence Sensor PDR

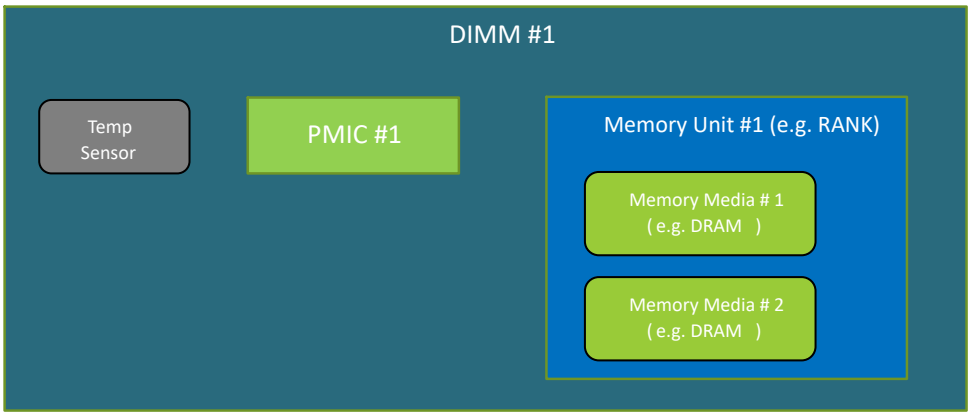
Table 17 — DIMM Presence Sensor PDR

Field	Value	Description
RecordHandle	4100	
SensorID	500	
EntityType	186	Slot
EntityInstance	1	
ContainerID	100	CMB #1
SensorType	13	Presence
PossibleStates	Refer to Table 1 of DSP0249	

274 ## 8.7 DIMM

275 The Memory Module refers to the DIMMs connected via DIMM Slots present in the CMB. Being a physical entity, the Memory Module is already declared within Figure 7. The content of the Memory Module includes a set of device-level sensors. The following diagram illustrates the model elements for the Memory Module in the example model:

276



277 **Figure 21 — Example model DIMM**

278 The Memory Module content is declared using an entity-association PDR that includes the hierarchical description of the Memory Module. The device-level sensors are declared with separate PDRs using direct references to the measured entities.

279

DIMM – Entity Association PDR		
Container ID	500	
Container Entity – DIMM #1		
Entity Type	144	Memory Module
Entity Instance Number	1	
ContainerID	400	DIMM Slot #1
Association Type	Physical to Physical containment	
Contained Entity 1 – PMIC #1		
Entity Type	124	DC-DC converter
Entity Instance Number	1	
ContainerID	500	Memory Module #1
Contained Entity 2 – Memory Chip #1		
Entity Type	142	Memory Chip
Entity Instance Number	1	
ContainerID	500	Memory Module #1
Contained Entity 3- Memory Chip #2		
Entity Type	142	Memory Chip
Entity Instance Number	2	
ContainerID	100	Memory Module #1

280 **Table 18 — DIMM Entity Association PDR**

281 ### 8.7.1 DIMM Temperature Sensor PDR

282 **Table 19 — DIMM Temperature Sensor PDR**

Field	Value	Description
RecordHandle	5100	
SensorID	600	

Field	Value	Description
EntityType	144	Memory Module
EntityInstance	1	
ContainerID	400	DIMM Slot #1
BaseUnit	2	Degrees C
UnitModifier	0	No need for scaling

283

9 ANNEX A (informative) Change Log

Version	Date	Description
1.0.0	5/21/2024	Initial Release